

UNIVERSITY OF REGINA
FACULTY OF ENGINEERING

EN 384 - Midterm Exam

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March 2, 1992
12:30 - 1:30



Marks (Total = 45)

- (10) Q1. The diode in circuit 1 is IDEAL.
- a) Develop the equations for the voltage transfer function (V_o vs V_i).
 - b) Specify the range of V_i that applies to each equation.
- (20) Q2. The transistor in circuit 2a is modelled by the characteristics in Fig. 2b.
- a) Select values of R_1 , R_2 , and R_L that will place the operating point of the circuit at location "A" (marked on Fig. 2b).
 - b) For the values you have selected above:
 - i) What range of input V_i will cause the transistor to be in the cutoff mode?
 - ii) What would the value of output voltage V_o be if the transistor "beta" was reduced to half of its original value?
- (15) Q3. The JFET in circuit 3a has the characteristics shown in Fig. 3b.
- a) Plot the voltage-current transfer characteristic for the JFET.
 - b) Plot the bias line for the circuit.
 - c) Plot the load line for the circuit.
 - d) Find the value of V_o .

4. Although some of the circuits in Fig. 4 are not practical, what basic logic functions (ie. NOT, OR etc.) are obtained at terminal Y?

5. An engineer is to design a circuit that will turn on and off a LED in response to an input voltage that is a sequence of rectangular pulses. She decides to use the circuit in Fig. 5. Her design is to be mass produced and must satisfy the following specifications:

...input voltage: rectangular pulses, $V_I(\text{low}) = 0 \text{ V}$
 $V_I(\text{high}) = 3 \text{ to } 5 \text{ V}$

...transistor beta: 50 to 300, (one design must work for all beta values since it is not practical to measure beta for each transistor and adjust design for each circuit produced)

...LED: $V_D(\text{on}) = 2 \text{ V}$, $I_D(\text{on}) = 10 \text{ to } 20 \text{ mA}$

Make the following simplifying assumptions:

- (1) transistor is ideal with constant beta over the full active region and $V_{CE}(\text{saturation}) = 0 \text{ V}$.
- (2) assume $I_D = I_C$ since beta is sufficiently large to ignore the contribution of I_B to LED current.
- (3) Your work will be easier if the operating range of the transistor is kept in the saturation region when the LED is on.

a) Complete the design by choosing values for R_B and R_C .

b) Are there minimum or maximum values for R_B and R_C that restricts your choice of values? If so specify the limits or range.

6. a) Name the logic family that:

- (1) has very low static power consumption.
- (2) generally has highest speed of operation. *CMOS*
- (3) tends to have highest power consumption. *BJT-ECL*
- (4) has the highest density of gates on an integrated circuit. *MOS*
- (5) generally has most limited fanout.
- (6) has best power-delay index of performance.

b) Explain the the term PN junction including: the materials used, how it is formed, how it works, the significance of minority and majority carriers and depletion region. Do not just copy words from the text.

Fanout
RTL 406
DTL 412
TTL 418
ECL - 43
MOS - 46