18 pages
ENEL

UNIVERSITY OF REGINA
FACULTY OF ENGINEERING

EN 384 FINAL EXAM
ENEL

INSTRUCTOR: K. J. RUNTZ 1992 April 20
2:00 - 5:00

MARKS: Q1 = 15 Q2 = 20 Q3 = 15 Q4 = 15
Q5 = 20 Q6 = 15 TOTAL = 100

1. The diodes in Fig. 1a have a forward voltage of Vo = 0.7 V but otherwise are ideal. The source, Vs, produces the triangular waveform in Fig. 1b.

a) Assume D1 is at the on/off transition state.
   i) What value is Vs?
   ii) In what state is D2? Prove it.
   iii) What value is VL?

if Vs - ve → reverse bias
if Vs + ve → forward bias

b) Assume Vs increases slightly above the value in (a).
   i) In what state is D1?
   ii) In what state is D2?
   iii) Derive an expression for VL as a function of Vs for the circuit in this state.

c) Plot the waveform for VL from t = 0 to 4.

2. The transistor in Figs. 2a and 2b has the characteristics in Fig. 2c.

a) On Fig. 2c, draw the load lines representing the operation of these circuits.

b) Mark the operating point of each circuit.

c) What effect (answer as increase, decrease, or nil) is there on ID and Vout if the following changes are made:

   (1) increase RG in 2a.
   (2) decrease RS in 2a.
   (3) increase RD in 2b.
   (4) decrease VDD in 2a.
   (5) decrease VDD in 2b.
   (6) increase VGG in 2a.
   (7) decrease RL in 2b.

3. Refer to the data sheet on page 670 of DeMassa. Assume only logic devices with the specifications of the 54 series are to be used in a system.

a) Calculate the maximum fanout.

b) Estimate the maximum frequency you could use to drive one of these gates.

c) If you design to the limits of these specifications, calculate the high and low noise margins.