2 pages

University of Regina

Faculty of Engineering

MidTerm ENEL **384** [redacted]

Digital Logic November 13, 1998

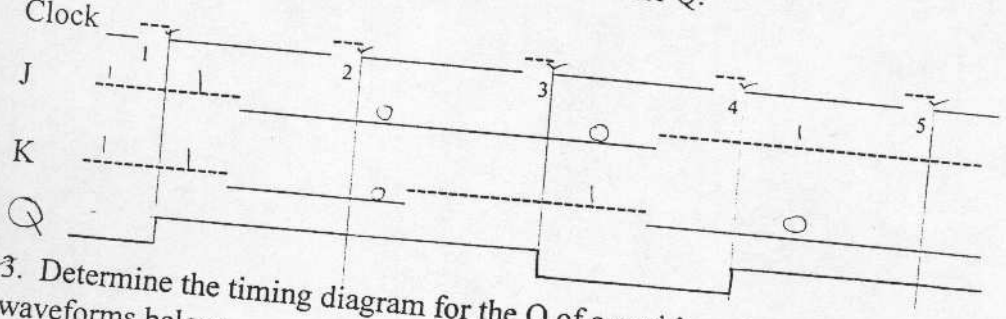
One 8x11 crib sheet allowed(original)
Questions are 20% each

R.J.Palmer

1. Design a MOD 12 asynchronous counter using JK flip-flops.

Jeremiah Worby

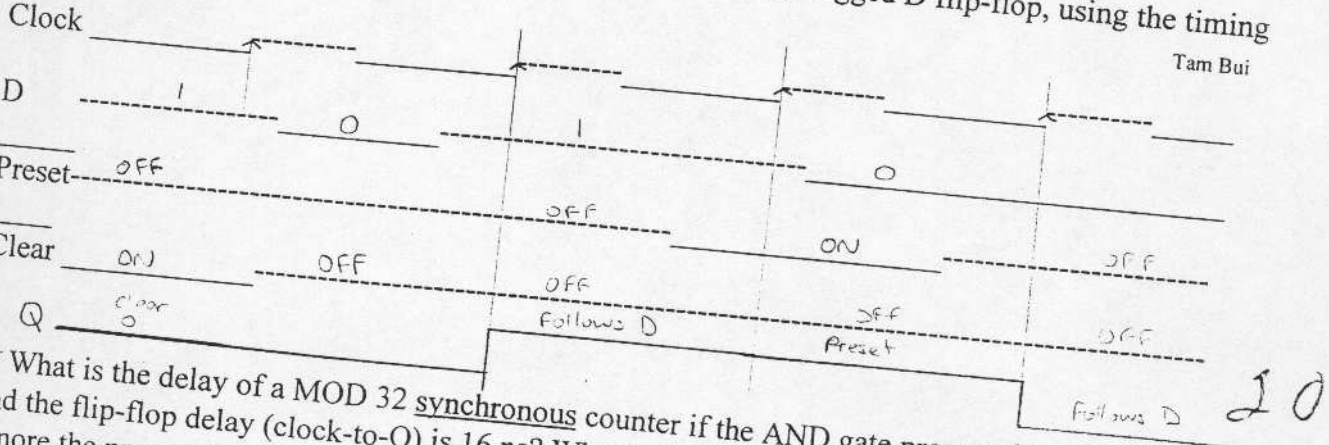
2. The waveforms below are applied to a negative edge triggered JK flip-flop initially in the RESET state. Determine the timing waveform for Q.



Zara

20

3. Determine the timing diagram for the Q of a positive edge trigged D flip-flop, using the timing waveforms below:



Tam Bui

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4. What is the delay of a MOD 32 synchronous counter if the AND gate propagation delay is 8 ns and the flip-flop delay (clock-to-Q) is 16 ns? What is the maximum clocking rate? Ignore the propagation delay of the routing.

Chad Delmuller

5. Design a **divide-by-40** using D flip-flops. Make the design synchronous.

Dave Nguyen

STUDENT I.D. NUMBER

1 – –

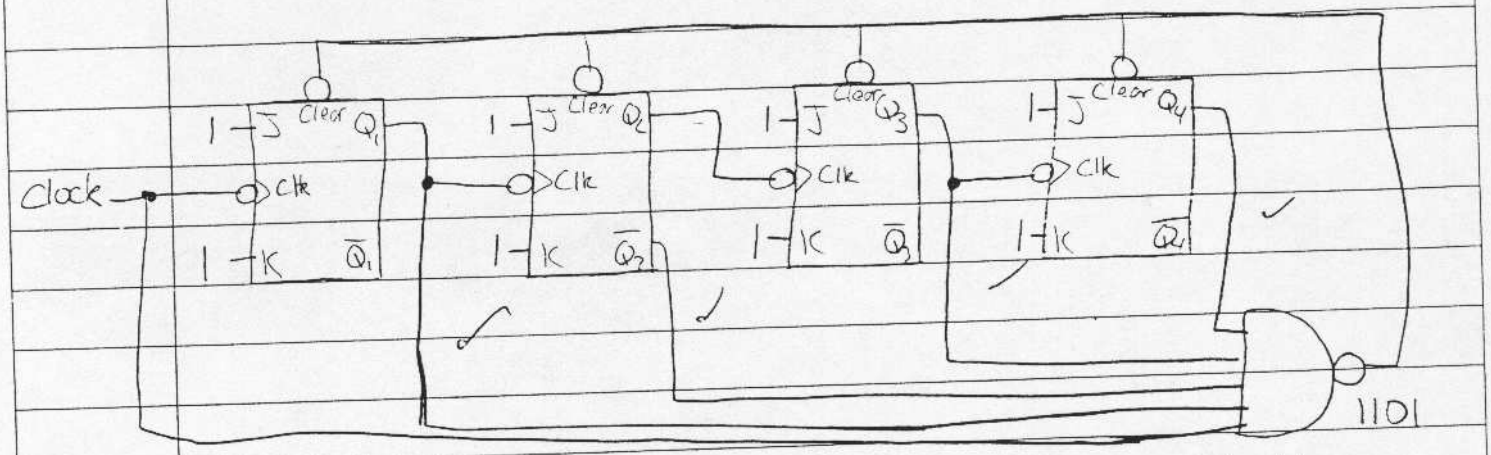
1. MOD 12 async. counter J-K FFs.

1000
1001
1010
1011
1100 ← 12
1101 ← 13

decode next state

1101
4 3 2 1

4 flip flops



- connect clock to NAND to prevent glitching

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